

ABSTRACT OF THE DISCLOSURE

The time and trouble of a mismatch cause analysis after logical equivalence verification can be reduced, and design and verification TAT can be shortened. A logical equivalence verifying device performs logical equivalence verification between two circuits, and displays the result of the logical equivalence verification. A preprocessing section 7 performs structural matching so as to determine whether there are portions corresponding in circuit structure to each other in corresponding logic cones of the two circuits. An internal DB 5 records the results of the structural matching as an identifier for each element. A subcone extracting section 8 extracts, as a subcone, a collection of elements, which are mutually to one another and have the same identifier, from each logic cone. A verifying section 9 performs logical equivalence verification between the two circuits for each of the extracted subcones. A display control section 10 displays only those subcones for which the logical equivalence verification has resulted in mismatch.